

SEMICONDUCTOR EQUIPMENT

CROSS REFERENCE TO RELATED APPLICATION

This application is based on Japanese Patent Applications No. 2002-316448 filed on October 30, 2002, and No. 2003-326508 filed 5 on September 18, 2003, the disclosures of which are incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to semiconductor equipment having a plurality of semiconductor devices and upper and lower layer 10 wirings.

BACKGROUND OF THE INVENTION

Semiconductor equipment 100 having a plurality of semiconductor devices 101 and upper and lower layer wirings according to a prior art is disclosed in Japanese Unexamined Patent 1.5 Application Publication No. H07-263665. As shown in Fig. 13, the semiconductor equipment 100 includes a plurality of laterally diffused metal oxide semiconductor (i.e., L-DMOS) transistors 101 having a source cell S and a drain cell D. The L-DMOS transistors 101 are arranged to have a mesh pattern. The first wiring layer 20 as the lower layer wiring is formed on the source and drain cells S, D through the first interlayer insulation film. Further, the second wiring layer as the upper layer wiring is formed on the first wiring layer through the second interlayer insulation film.

The lower layer wiring is composed of a plurality of the first

source wirings 1 and a plurality of the first drain wirings 2. Each first source wiring 1 connects to a plurality of the source cells S, which are aligned in a diagonal direction of the mesh pattern. Each first drain wiring 2 connects to a plurality of the drain cells 5 D, which are also aligned in the diagonal direction. The first source wirings 1 and the first drain wirings 2 are aligned alternately. The upper layer wiring is composed of the second source wiring 3 and the second drain wiring 4. The second source wiring 3 connects to a plurality of first source wirings 1 through 10 contact portions (not shown) disposed under the second source wiring 3, and the second drain wiring 4 connects to a plurality of first drain wirings 2 through contact portions (not shown) disposed under the second drain wiring 4. The second source wiring 3 and the second drain wiring 4 almost equally divide the semiconductor equipment 15 100, and each of them has a triangle shape.

Since the wirings for connecting each cell in the L-DMOS transistor 101 are formed into double layered structure, i.e., formed into the upper and lower layer wirings, so that an occupation area of the upper and lower layer wirings is reduced. Moreover, 20 each cell can be minimized, so that a chip size of the semiconductor equipment 100 is reduced.

Each of the second source and drain wirings 3, 4 as the upper layer wiring has a wide area so that the electric resistance of the upper layer wiring as a wiring resistance is suppressed. Further, 25 each wide area of the upper layer wiring can be used as a pad region for forming a solder bump. Therefore, the semiconductor equipment 100 can be mounted on a ceramic circuit board or a printed circuit

board so that the semiconductor equipment 100 is packaged into a chip size package (i.e., CSP). Therefore, a mounting area of the semiconductor equipment 100 is reduced.

However, each of the source and drain cells S, D connecting 5 to the lower layer wirings is affected by the wiring resistance differently. For example, a source cell B shown in Fig. 13, which is disposed under the second source wiring 3, connects to the second source wiring 3 at a right above contact portion. Therefore, the source cell B is not affected by the wiring resistance of the first 10 source wiring 1 substantially. A source cell C shown in Fig. 13 is disposed under the second drain wiring 4, i.e., the source cell C is not disposed under the second source wiring 3. Therefore, the source cell C is far from a contact portion between the first source wiring 1 and the second source wiring 3, so that the source cell 15 C is much affected by the wiring resistance of the first source wiring 1. In other words, current flowing from the source cell C passes through the first source wiring 1, which is narrow and has a long path.

The above different affection of the wiring resistance breaks 20 down the balance of current flowing through each cell. For example, the current concentrates on the source cell B, and the current does not flow through the source cell C substantially, so that the total withstand voltage of the semiconductor equipment 100 is reduced.

SUMMARY OF THE INVENTION

25 In view of the above problem, it is an object of the present invention to provide semiconductor equipment having a plurality of

semiconductor devices and upper and lower layer wirings. Specifically, the semiconductor equipment has a plurality of semiconductor devices, in which current flows homogeneously so that the semiconductor equipment has a high withstand voltage.

5 It is another object of the present invention to provide semiconductor equipment having homogeneous current distribution, which can be packaged into a chip size package.

Semiconductor equipment includes a semiconductor substrate, a plurality of transistors having a source cell and a drain cell 10 disposed alternately on the substrate so as to form a mesh pattern, and upper and lower layer wirings for electrically connecting the source cells and the drain cells. The lower layer wiring includes a first source wiring having a striped shape for connecting the neighboring source cells and a first drain wiring having a striped 15 shape for connecting the neighboring drain cells. The upper layer wiring includes a second source wiring having a striped shape for connecting to the first source wiring and a second drain wiring having a striped shape for connecting to the first drain wiring. The second source wiring has a width of a stripe, which is wider 20 than that of the first source wiring, and the second drain wiring has a width of a stripe, which is wider than that of the first drain wiring. The second source wiring and the second drain wiring are disposed alternately.

In the above equipment, a contact portion between the lower 25 layer wiring and the upper layer wiring is disposed alternately and homogeneously on the substrate. Accordingly, current path of the lower layer wiring having narrow striped shape becomes short.

Therefore, the wiring resistance of the lower layer wiring does not affect to the transistor substantially. Thus, the current flows in each cell homogeneously so that the semiconductor equipment has a high withstand voltage. Moreover, the semiconductor equipment 5 has homogeneous current distribution, so that the equipment can be packaged into a chip size package.

Preferably the first drain wiring has a minimum width of the stripe, which is narrower than that of the first source wiring. In this case, the contact portion between the drain cell and the first 10 drain wiring can become smaller than the contact portion between the source cell and the first source wiring. Therefore, the minimum width of the first drain wiring becomes narrower than the minimum width of the first source wiring, so that the current path is optimized in accordance with the size of the contact portion. Thus, 15 the wiring resistance of the lower layer wiring is reduced.

Further, semiconductor equipment includes a semiconductor substrate, a plurality of lateral type metal oxide semiconductor transistors having a source cell and a drain cell, which are disposed alternately on a principal plane of the substrate so as to form a 20 mesh pattern, and upper and lower layer wirings disposed on the substrate for electrically connecting the source cells and the drain cells. The lower layer wiring includes a first drain wiring for connecting the neighboring two drain cells disposed in a diagonal direction of the mesh pattern, and a first source wiring for 25 connecting the source cells and surrounding the first drain wiring. The upper layer wiring includes a second source wiring disposed perpendicularly to the first source wiring and having a striped shape

for connecting to the first source wiring through a source via-hole, and a second drain wiring disposed perpendicularly to the first drain wiring and having a striped shape for connecting to the first drain wiring through a drain via-hole. The second source wiring has a 5 width of a stripe, which is wider than a minimum width of a stripe of the first source wiring, which is disposed between the neighboring first drain wirings, and the second drain wiring has a width of a stripe, which is wider than a minimum width of a stripe of the first drain wiring. The second source wiring and the second drain wiring 10 are disposed alternately.

In the above equipment, the wiring resistance of the lower layer wiring does not affect to the transistor substantially. Thus, the current flows in each cell homogeneously so that the semiconductor equipment has a high withstand voltage. Moreover, 15 the semiconductor equipment has homogeneous current distribution, so that the equipment can be packaged into a chip size package. Further, the area of the first source wiring is larger than the area of the first drain wiring, so that the source current flowing through the source cell flows mainly in the lower layer wiring. On the other 20 hand, the drain current flowing through the drain cell flows mainly in the upper layer wiring. Thus, the source and drain currents are distributed by the lower and upper layer wirings, respectively, so that degree of freedom of wiring pattern becomes large. Thus, the total wiring resistance is much reduced.

25 Further, semiconductor equipment includes a semiconductor substrate, a plurality of lateral type metal oxide semiconductor transistors having a source cell and a drain cell, which are disposed

alternately on a principal plane of the substrate so as to form a mesh pattern, and upper and lower layer wirings disposed on the substrate for electrically connecting the source cells and the drain cells. The lower layer wiring includes a first source wiring for 5 connecting the neighboring two source cells disposed in a diagonal direction of the mesh pattern, and a first drain wiring for connecting the drain cells and surrounding the first source wiring. The upper layer wiring includes a second source wiring disposed perpendicularly to the first source wiring and having a striped shape 10 for connecting to the first source wiring through a source via-hole, and a second drain wiring disposed perpendicularly to the first drain wiring and having a striped shape for connecting to the first drain wiring through a drain via-hole. The second source wiring has a width of a stripe, which is wider than a minimum width of a stripe 15 of the first source wiring, which is disposed between the neighboring first drain wirings, and the second drain wiring has a width of a stripe, which is wider than a minimum width of a stripe of the first drain wiring. The second source wiring and the second drain wiring are disposed alternately.

20 In the above equipment, the current flows in each cell homogeneously so that the semiconductor equipment has a high withstand voltage. Moreover, the semiconductor equipment has homogeneous current distribution, so that the equipment can be packaged into a chip size package. Further, the source and drain 25 currents are distributed by the lower and upper layer wirings, respectively, so that degree of freedom of wiring pattern becomes large. Thus, the total wiring resistance is much reduced.

Furthermore, semiconductor equipment includes a semiconductor substrate, a plurality of transistors having a source cell and a drain cell, which are disposed alternately on a principal plane of the substrate so as to form a mesh pattern, a lower layer 5 wiring disposed on the source and drain cells and including a first source wiring for connecting the source cells and a first drain wiring for connecting the drain cells, and an upper layer wiring disposed on the lower layer wiring and including a second source wiring for connecting to the first source wiring through a source 10 via-hole and a second drain wiring for connecting to the first drain wiring through a drain via-hole. At least one of the source and drain via-holes has a predetermined pattern so that a length of periphery of the via-hole becomes maximum.

In the above equipment, the wiring resistance between the 15 first source or drain wiring and the second source or drain wiring through the via-hole becomes small, so that the semiconductor equipment has a high withstand voltage.

Preferably, at least one of the source and drain via-holes has a plurality of small via-holes. In this case, the total length 20 of the periphery of the via-hole becomes larger than that of a via-hole having merely one via-hole. Therefore the wiring resistance at the via-hole is reduced.

Preferably, at least one of the source and drain via-holes has a ring shape. In this case, an inner circumference of the 25 via-hole is added with an outer circumference of the via-hole, so that the total length of the periphery of the via-hole becomes long. Thus, the wiring resistance at the via-hole is reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description made with reference to the accompanying 5 drawings. In the drawings:

Fig. 1 is a schematic plan view showing semiconductor equipment according to a first embodiment of the present invention;

Fig. 2 is a plan view explaining an arrangement of a lower layer wiring of the semiconductor equipment according to the first 10 embodiment;

Fig. 3 is a plan view explaining a contact portion between upper and lower layer wirings of the semiconductor equipment according to the first embodiment;

Fig. 4 is a partially enlarged cross-sectional view showing 15 a L-DMOS transistor of semiconductor equipment according to the first embodiment;

Fig. 5 is a schematic plan view explaining a CSP arrangement, according to the first embodiment;

Fig. 6 is a schematic plan view explaining another CSP 20 arrangement according to the first embodiment;

Fig. 7A is a partially enlarged plan view of a region A in Fig. 3, and Fig. 7B is a cross-sectional view taken along line VIIIB-VIIB in Fig. 7A;

Fig. 8 is a partially enlarged plan view of the region A in 25 Fig. 3 showing a plurality of via-holes, according to the first embodiment;

Figs. 9A-9D are plan views showing various via-holes,

according to a modification of the first embodiment;

Fig. 10 is a plan view explaining an arrangement of a lower layer wiring of semiconductor equipment according to a second embodiment of the present invention;

5 Fig. 11 is a plan view explaining a contact portion between upper and lower layer wirings of the semiconductor equipment according to the second embodiment;

Fig. 12 a plan view explaining another arrangement of the lower layer wiring of the semiconductor equipment according to the second 10 embodiment; and

Fig. 13 is a schematic plan view showing semiconductor equipment according to a prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

15 Semiconductor equipment 200 according to a first embodiment of the present invention is shown in Figs. 1-4. The semiconductor equipment 200 includes a lateral type metal oxide semiconductor (i.e., lateral type MOS) transistor such as a L-DMOS transistor.

As shown in Fig. 4, the L-DMOS transistor is formed on a 20 semiconductor substrate having an N type semiconductor layer 10. On a surface portion of the semiconductor layer 10, a P type channel diffusion region 11 is formed. The channel diffusion region 11 terminates almost at an end of a local oxidation of silicon (i.e., LOCOS) region 5. On a surface portion of the channel diffusion 25 region 11, a N⁺ type source diffusion region 12 is formed so as to separate from the LOCOS region 5. Further, on the surface portion

of the channel diffusion region 11, a P⁺ type diffusion region 15 is formed so as to contact the source diffusion region 12.

On the surface portion of the semiconductor layer 10, a N⁺ type drain diffusion region 13 is formed so as to contact the LOCOS region 5. The drain diffusion region 13 is a heavy doped region, i.e., a high concentration region. An N type well region 16 is formed so as to surround the drain diffusion region 13 and the LOCOS region 5. A gate electrode 14 is formed on the surface of the channel diffusion region 11 through a gate insulation film (not shown), which 10 is disposed between the source diffusion region 12 and the LOCOS region 5.

The gate electrode 14 is covered with the first interlayer insulation film 6. On the first interlayer insulation film 6, the first source wiring 1 as a lower layer wiring and the first drain wiring 2 as a lower layer wiring are formed. The first source wiring 1 connects to the source diffusion region 12 and the diffusion region 15 through a contact hole of the first interlayer insulation film 6, i.e., the first source wiring 1 connects to a source of the L-DMOS transistor through the contact hole. The first drain wiring 2 connects to the drain diffusion region 13 through the other contact hole of the second interlayer insulation film 7, i.e., the first drain wiring 2 connects to a drain of the L-DMOS transistor through the other contact hole. The second drain wiring 4 is formed through the third contact hole disposed in the second interlayer insulation 20 film 7, i.e., the second drain wiring 4 connects to the drain diffusion region 13 through the third contact hole disposed in the second interlayer insulation film 7.

Thus, the lateral type MOS transistor includes a source cell S disposed on the left side in Fig. 4 and a drain cell D disposed

on the right side in Fig. 1. Fig. 2 shows a cell arrangement of the semiconductor equipment 200, and a contact portion between the cell and the lower layer wiring. Fig. 3 shows the lower layer wiring of the semiconductor equipment 200. Fig. 4 shows the upper layer 5 wiring and its contact portion between the upper and lower layer wirings.

As shown in Fig. 1, a principal plane of the semiconductor substrate of the semiconductor equipment 200 is patterned into a square mesh pattern. The source cell S or the drain cell D of the 10 lateral type MOS transistor is formed into a unit cell of the square mesh pattern. In Fig. 1, each source cell 20S, 20SE has a large contact portion 21S for connecting between the source of the lateral type MOS transistor and the lower layer wiring. The drain cell 20D has a small contact portion 21D for connecting between the drain 15 of the transistor and the lower layer wiring.

In the semiconductor equipment 200, the source cell 20SE is disposed on a periphery of the mesh pattern so that the source cell 20SE surrounds the inner mesh pattern. The source cell 20S and the drain cell 20D are disposed on the inner mesh pattern alternately. 20 This is because the source cell 20SE stably operated in lower electric potential surrounds the drain cell 20D so that the semiconductor equipment 20 is stably operated. Even when the semiconductor equipment 200 includes a trench for insulating and surrounding the mesh pattern having the source and drain cells 20S, 25 20SE, 20D of the transistor, a high voltage between the source and drain cells 20SE, 20D is not applied to the edge of the trench. Therefore, the electric potential of the edge of the trench can be

stabilized so that current leakage or dielectric breakdown at the trench is suppressed. Here, the leakage or the breakdown is, for example, caused by a crystal defect disposed on the edge of the trench. However, the drain cell 20D can be disposed on the periphery of the
5 mesh pattern.

Fig. 2 shows the lower layer wiring disposed on the mesh pattern. The lower layer wiring is composed of the first source wiring 1 and the first drain wiring 2, which are disposed alternately, and each of them has a striped pattern. The first source wiring
10 1 connects to the source cells 20S, 20SE disposed in a diagonal direction of the mesh pattern. The first drain wiring 2 connects to the drain cells disposed in the diagonal direction of the mesh pattern.

Fig. 3 shows the upper layer wiring and its contact portion
15 between the upper and lower layer wirings disposed on the lower layer wiring. The upper layer wiring is composed of the second source and drain wirings 3, 4 disposed perpendicularly to the first source and drain wirings 1, 2. The second source wiring 3 connects to the first source wiring 1 through a via-hole 30. The second drain wiring
20 4 connects to the first drain wiring 2 through a via-hole 40. Each of the second source and drain wirings 3, 4 has a striped pattern, respectively. Each width of the stripe of the second source and drain wirings 3, 4 is wider than that of the first source and drain wirings 1, 2. The second source and drain wirings 3, 4 are disposed
25 alternately. Each of the second source and drain wirings 3, 4 includes a connection portion 3R, 4R for connecting a plurality of stripes so that it forms a comb shaped wiring. Therefore, each

stripe as a tooth of comb of the second source and drain wirings 3, 4 faces each other. Thus, each of the source and drain cells 20S, 20D electrically connects in parallel, respectively.

As described above, the striped first source and drain wirings 5 1, 2 are disposed alternately on the source and drain cells S, D having the mesh pattern so that the same type of cells disposed in the diagonal direction of the mesh pattern are connected together. The striped second source and drain wirings 3, 4 are disposed perpendicularly to the first source and drain wirings 1, 2, and 10 disposed alternately thereon, so that the second source and drain wirings 3, 4 connect to the first source and drain wirings 1, 2 through the via-holes 30, 40, respectively. Therefore, each cross-section, i.e., each contact portion between the first and third source wirings 1, 3 and between the first and second drain 15 wirings 2, 4 is disposed alternately, so that each of the via-holes 30, 40 is disposed on the contact portion, respectively.

Therefore, current path in the first source and drain wiring 1, 2 can become short, so that the influence of the wiring resistance of the lower layer wiring for affecting to each of the source and 20 drain cells S, D becomes small. The current flows in each cell homogeneously so that the semiconductor equipment 200 has a high withstand voltage. Moreover, the first and second source wirings 1, 3 or the first and second drain wirings 2, 4 electrically connect to the source or drain cells 20S, 20D, respectively. Therefore, 25 each connection portion 3R, 4R of the second source and drain wirings 3, 4 can have a predetermined area so that the connection portion 3R, 4R is used as a pad region for forming a solder bump. Thus,

the semiconductor equipment 200 can be mounted on a ceramic board or a printed circuit board so that the semiconductor equipment 200 is packaged into a chip size package (i.e., CSP). Thus, a mounting area of the semiconductor equipment 200 is reduced.

5 In this case, the third layer wiring for the CSP can be formed on the upper layer wiring, as shown in Figs. 5 and 6. Semiconductor equipments 201, 202 have the third layer wirings, each of which is composed of the third source wiring 8S, 9S and the third drain wiring 8D, 9D. The third source wiring 8S, 9S connects to the second source 10 wiring 3, and the third drain wiring 8D, 9D connects to the second drain wiring 4. In the semiconductor equipment 201, the third source and drain wirings 8S, 8D divide the semiconductor equipment 201 in quarters, and each of them has a rectangular shape. In the semiconductor equipment 202, the source and drain wirings 9S, 9D 15 divide the semiconductor equipment 202 in two parts, and each of them has a triangle shape. Here, a via-hole (not shown) connects the third source wiring 8S, 9S and the second source wiring 3, and another via-hole (not shown) connects the third drain wiring 8D, 9D and the second drain wiring 4. These via-holes can be formed 20 on a predetermined position. Since the second source and drain wirings 3, 4 have a plurality of stripes with wide width, the influence of the wiring resistance is reduced.

Both the third source wiring 8S, 9S and the third drain wiring 8D, 9D have wide areas shown in Figs. 4 and 5. Therefore, a pad 25 region can be formed on a predetermined position of the above wide area, so that the semiconductor equipment 201, 202 is packaged into a CSP.

Further, the semiconductor equipment 201, 202 has no connection portion 3R, 4R shown in Fig. 3. In other words, the third source and drain wirings 8S, 9S, 8D, 9D instead of the connection portion 3R, 4R connect the second source or drain wiring 3, 4 together. 5 Thus, the source cell 20S or the drain cell 20D electrically connects together in parallel by using the second source or drain wiring 3, 4 with the third source and drain wirings 8S, 9S, 8D, 9D.

Fig. 7A is a partially enlarged plan view showing an area A shown in Fig. 3. Fig. 7B is a cross-sectional view taken along line 10 VIIB-VIIB in Fig. 7A. Each of the via-holes 30, 40 connects the thin first source or drain wiring 1, 2 and the thick second source or drain wiring 3, 4, respectively. A metallic film in the via-hole 30, 40 is simultaneously formed together with the second source and drain wirings 3, 4. A film thickness TV of the metallic film disposed 15 on a sidewall of the via-hole 30, 40 is thinner than a film thickness TA of the second source and drain wirings 3, 4. In this case, current flowing through the metallic film in the via-hole 30, 40 is limited by the film thickness TV disposed on the sidewall of the via-hole 30, 40. Therefore, a cross-section of the current passing through 20 the metallic film in the via-hole 30, 40 becomes larger, as the peripheral length of the via-hole 30, 40 becomes large. Therefore, it is preferred that the peripheral length of the via-hole 30, 40 becomes longer.

For example, a preferred via-hole 30W, 40W is shown in Fig. 25 8. Each via-hole 30W, 40W has six small via-holes disposed in one contact portion 21S, 21D between the first source or drain wiring 1, 2 and the second source or drain wiring 3, 4. Therefore, the

total peripheral length of the via-hole 30W, 40W becomes longer than that of the via-hole 30, 40, so that the wiring resistance at the via-hole 30W, 40W is reduced. Although the via-hole 30W, 40W has six small via-holes, the via-hole 30W, 40W can have another number 5 of small via-holes, which is predetermined in accordance with an area of the contact portion 21S, 21D between the first source or drain wiring 1, 2 and the second source or drain wiring 3, 4.

Figs. 9A to 9D show various via-holes having different patterns. These via-holes have the same gross area. As shown in 10 Fig. 9A, a via-hole HA has one large rectangular shaped via-hole. A via-hole HB shown in Fig. 9B has six square via-holes, the total peripheral length of the via-hole HB is about half time longer than that of the via-hole HA. In this case, the wiring resistance of the via-hole 15 HC shown in Fig. 9C has a ring shaped via-hole, the total peripheral length of the via-hole HC is about half time longer than that of the via-hole HA. In this case, the wiring resistance of the via-hole HC is two thirds of that of the via-hole HA. A via-hole HD shown in Fig. 9D has eight square via-holes, the total peripheral length 20 of the via-hole HD is about twice longer than that of the via-hole HA. In this case, the wiring resistance of the via-hole HD is one-half of that of the via-hole HA.

Further, the sidewall of the via-hole 30, 40 can be formed into a tapered shape so that the metallic film disposed on the 25 sidewall of the via-hole 30, 40 becomes thicker. The metallic film can be easily deposited on the sidewall of the via-hole 30, 40 having the tapered shape, so that the metallic film in the via-hole 30,

40 having the tapered shape is deposited thicker than that in the via-hole 30, 40 without any tapered shape is deposited. Thus, the wiring resistance of the via-hole 30, 40 having the tapered shape is reduced.

5 (Second Embodiment)

Semiconductor equipment 300 according to a third embodiment of the present invention is shown in Figs. 10 and 11. Fig. 10 shows the lower layer wiring of the semiconductor equipment 300. Fig. 11 shows the upper layer wiring and its contact portion between the upper and lower layer wirings. As shown in Fig. 10, the lower layer wiring is composed of the first drain wirings 2A, 2B and the first source wiring 1A. Each first drain wiring 2A, 2B connects neighboring two, three or four drain cells 20D disposed in the diagonal direction of the mesh pattern. The first source wiring 1A surrounds the first drain wirings 2A, 2B, and connects all the source cells 20S, 20SE. Here, the first drain wirings 2A, 2B is categorized into two groups according to the mesh pattern. One is the first drain wiring 2A, which is not adjacent to the source cell 20SE disposed on the periphery of the mesh pattern. The first drain wiring 2A connects two drain cells 20D disposed on the inner mesh pattern. The other is the first drain wiring 2B, which is adjacent to the source cell 20SE disposed on the periphery of the mesh pattern. The first drain wiring 2B connects two, three or four drain cells 20D.

25 As shown in Fig. 11, the second source and drain wirings 3A, 4A have a plurality of corrugated stripes, function of which are almost equal to the stripes of the second source and drain wirings

3, 4 shown in Fig. 3. The second drain wiring 4A connects to the first drain wirings 2A, 2B through a via-hole 40A. The second source wiring 3A connects to the first source wirings 1A through a via-hole 30A. Each width of the stripes of the second source and drain wirings 5 3A, 4A is wider than the minimum width of the stripes of the first source and drain wirings 1A, 2A, respectively. Here, the minimum width of the stripes of the first source wiring 1A is the width of the first source wiring 1A disposed between the stripes of the first drain wirings 2A. Each stripes of the first source and drain wirings 10 1A, 2A is connected by a connection portion 3RA, 4RA, so that the first source or drain wirings 1A, 2A has a comb shape. Thus, the source cell 20S, 20SE or the drain cell 20D is electrically connected together in parallel by both the first source or drain wiring 1A, 2A, 2B and the second source or drain wiring 3A, 4A, respectively.

15 In the semiconductor equipment 300, the current path of the first source and drain wirings 1A, 2A, 2B having narrow width becomes short, so that the influence of the wiring resistance of the first source and drain wirings 1A, 2A, 2B is reduced. Therefore, the current flows in each cell 20S, 20SE, 20D homogeneously so that the 20 semiconductor equipment 300 has a high withstand voltage.

Although the gross area of the first source wiring 1 shown in Fig. 2 is almost equal to that of the first drain wiring 2, the gross area of the first source wiring 1A shown in Fig. 10 is larger than that of the first drain wiring 2A, 2B. Therefore, the wiring 25 resistance of the first source wiring 1A is reduced, so that the source current flows mainly in the first source wiring 1A. On the other hand, the drain current flows mainly in the second drain wiring

4A, since the gross area of the first drain wirings 2A, 2B is small. Thus, the current flowing through the drain cell 20D mainly flows in the upper layer wiring, and the current flowing through the source cell 20S, 20SE of the L-DMOS transistor mainly flows in the lower 5 layer wiring, so that the degree of freedom of patterning of the upper and lower wirings increases. Further, the total wiring resistance is reduced. Especially, when the semiconductor equipment 300 further includes another CMOS transistor or a bipolar transistor, the lower layer wiring made of aluminum is required to 10 become downsized, for example, the thickness of the lower layer wiring is limited to be equal to or smaller than $0.7 \mu\text{m}$. On the other hand, the width of the upper layer wiring may be large, so that the thickness of the upper layer wiring is, for example, $1.3 \mu\text{m}$. Accordingly, the semiconductor equipment 300 having the lower layer 15 wirings 1A, 2A, 2B can provide to become downsized and to reduce the wiring resistance.

Further, each connection portion 3RA, 4RA of the second source and drain wirings 3A, 4A can have a predetermined area so that the connection portion 3RA, 4RA is used as a pad region for forming a 20 solder bump. Thus, the semiconductor equipment 300 can be mounted on a ceramic board or a printed circuit board so that the semiconductor equipment 300 is packaged into a CSP. Thus, a mounting area of the semiconductor equipment 300 is reduced.

Further, the third layer wiring can be formed on the upper 25 layer wiring, i.e., the second source and drain wiring 3A, 4A so that the semiconductor equipment 300 is packaged into the CSP. Furthermore, each via-hole 30A, 40A between the lower layer wiring

and the upper layer wiring can be formed into a predetermined pattern such as the via-holes 30W, 40W, HA, HB, HC, HD shown in Figs. 7 and 8A-8D.

Another semiconductor equipment 301 according to a modification of the second embodiment is shown in Fig. 12. The semiconductor equipment 300 shown in Fig. 10 has the lower layer wiring, i.e., the first source and drain wirings 1A, 2A, 2B with the corrugated shapes, i.e., with concavity and convexity portions so as to become wider. Thus, a portion of the lower layer wiring around the contact portion is wider than the minimum width of the lower layer wiring. However, the semiconductor equipment 301 has the first source and drain wirings 1B, 2C, 2D with a straight striped shape. Specifically, the minimum width of the first drain wiring 2C, 2D is narrower than that of the first source wiring 1B disposed between the neighboring first drain wirings 2C, 2D.

In the semiconductor equipment 301, for example, the current flowing through the drain cell 20D can mainly flow in the upper layer wiring, and the current flowing through the source cell 20S, 20SE of the L-DMOS transistor can mainly flow in the lower layer wiring, so that the degree of freedom of patterning of the upper and lower wirings increases. Therefore, the total wiring resistance is much reduced. Further, the current path of the upper and lower layer wirings have no concavity and convexity portion in accordance with the size of the contact portion, so that the total wiring resistance is further reduced.

(Modification)

Although the source cell 20SE is disposed on the periphery

of the mesh pattern, the drain cell can be disposed on the periphery of the mesh pattern. Further the drain cell can surround the inner mesh pattern, which is composed of the source cell and drain cell alternately disposed. In this case, as shown in Fig. 1, even when 5 a trench is formed so as to surround the mesh pattern for insulating the semiconductor equipment, the trench does not cut a PN junction. Therefore, the current leakage is limited from being occurred. Specifically, assuming that the trench is disposed on the left side of the source cell and the right side of the drain cell, a PN junction 10 between the N type semiconductor layer 10 and the P type channel diffusion region 11 contacts the trench disposed on the left side of the source cell. On the other hand, in the trench disposed on the right side of the drain cell, an interface between the N type semiconductor layer 10 and the N⁺ type well region 16 does not form 15 the PN junction. Therefore, when the drain cell is disposed on the periphery of the mesh pattern, the PN junction does not disposed on the periphery of the mesh pattern so that the current leakage or the insulation break down, which are caused by cutting the PN junction by the trench, is limited from being occurred. Here, when 20 the drain cell is disposed on the periphery of the mesh pattern and the source and drain cells are disposed alternately in the inner mesh pattern, the relationship between the upper and lower layer wirings according to the source and drain cells is reversed.

Such changes and modifications are to be understood as being 25 within the scope of the present invention as defined by the appended claims.